CLAIMS:

1. A differential amplifier (1) for amplifying an input differential signal having two components (In^+, In^-) substantially in anti-phase to each other and generating an output differential signal having two differential components (Out^+, Out^-), said amplifier (1) comprising a pair of inverters (10) coupled to a pair of adders (30) the inverters (10) receiving the input differential signal, the amplifier (1) being characterized in that it further comprises a pair of controllable buffers (20) for receiving the input differential signal and outputting a signal to the pair of adders (30), a bias of the said pair of buffers being cross-controlled by the input differential signal for controlling an amplification of said pair of controllable buffers (20).

2. A differential amplifier (1) as claimed in Claim 1, wherein the pair of inverters (10) and the pair of controllable buffers (20) are voltage to current converters.

3. A differential amplifier (1) as claimed in Claim 2, wherein the pair of adders (30) comprises a series combination of resistive means (R, xR).

4. A differential amplifier (1) as claimed in Claim 2 – 3, wherein the differential amplifier (1) is coupled to a current to voltage converter (100) for adapting a current type differential input signal (C^+, C^-) to a voltage type differential signal (In^+, In^-) said voltage being inputted to the differential amplifier (1).

5. A differential amplifier (1) as claimed in Claim 2, wherein the pair of inverters (10) comprises a pair of common-emitter coupled transistors (T1, T2).

6. A differential amplifier (1) as claimed in Claim 3, wherein the pair of controllable buffers (20) comprises a pair of common-base transistors (T3, T4).

7. A differential amplifier (1) as claimed in Claim 6, wherein the pair of common-base transistors are cross-coupled to the differential input signal via capacitive means (40) for removing a DC component included in the differential input signal.

8. A differential amplifier (1) as claimed in Claim 6, wherein the pair of common-emitter transistors (T1, T2) has a first feedback means (R1) for controlling an amplification of said pair of transistors (T1, T2).

9. A differential amplifier (1) as claimed in Claim 7, wherein the pair of common-base transistors (T3, T4) comprises a pair of second feedback means (R2) for adapting an input impedance of the pair of common-base transistors (T3, T4) to an output impedance of a generator, said generator transmitting the differential input signal.

10. A receiver (500) comprising a differential amplifier (1) as claimed in claims 1 – 9.